AMENDMENTS TO THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-23. (Cancelled).

24. (New) A system for sharing interrupt controller inputs, said system comprising:

K input sources, wherein K is an integer value;

an interrupt controller having N inputs, wherein N is an integer value less than K;

N logical mapping subsets corresponding to the N inputs of the interrupt controller, said logical mapping subsets including:

- K logical ANDs having respective first inputs, second inputs and outputs, said first inputs being coupled to the K input sources, respectively,
- a logical OR having a plurality inputs coupled to the output of the K logical ANDs within the respective logical mapping subset, and an output coupled to the corresponding input of the interrupt controller; and

N control bit sets corresponding to the N logical mapping subsets, respectively, said control bit sets having K control bits coupled to the second input of the K logical ANDs in the corresponding logical mapping subset.

25. (New) The system of claim 24, further comprising a register for storing the control bit values.

26. (New) The system of claim 24, further comprising logic that sets the control bit values according to user preferences.

27. (New) The system of claim 26, further comprising logic that dynamically modifies the control bit values according to user preferences.

28. (New) The system of claim 24, further comprising logic that defines the control bit values according to system requirements, said system comprising the processor, at least one interrupt source, and at least one interrupt input.

29. (New) The system of claim 24, wherein the processor is part of a microcontroller unit.